



FIG. 1

Power Settings

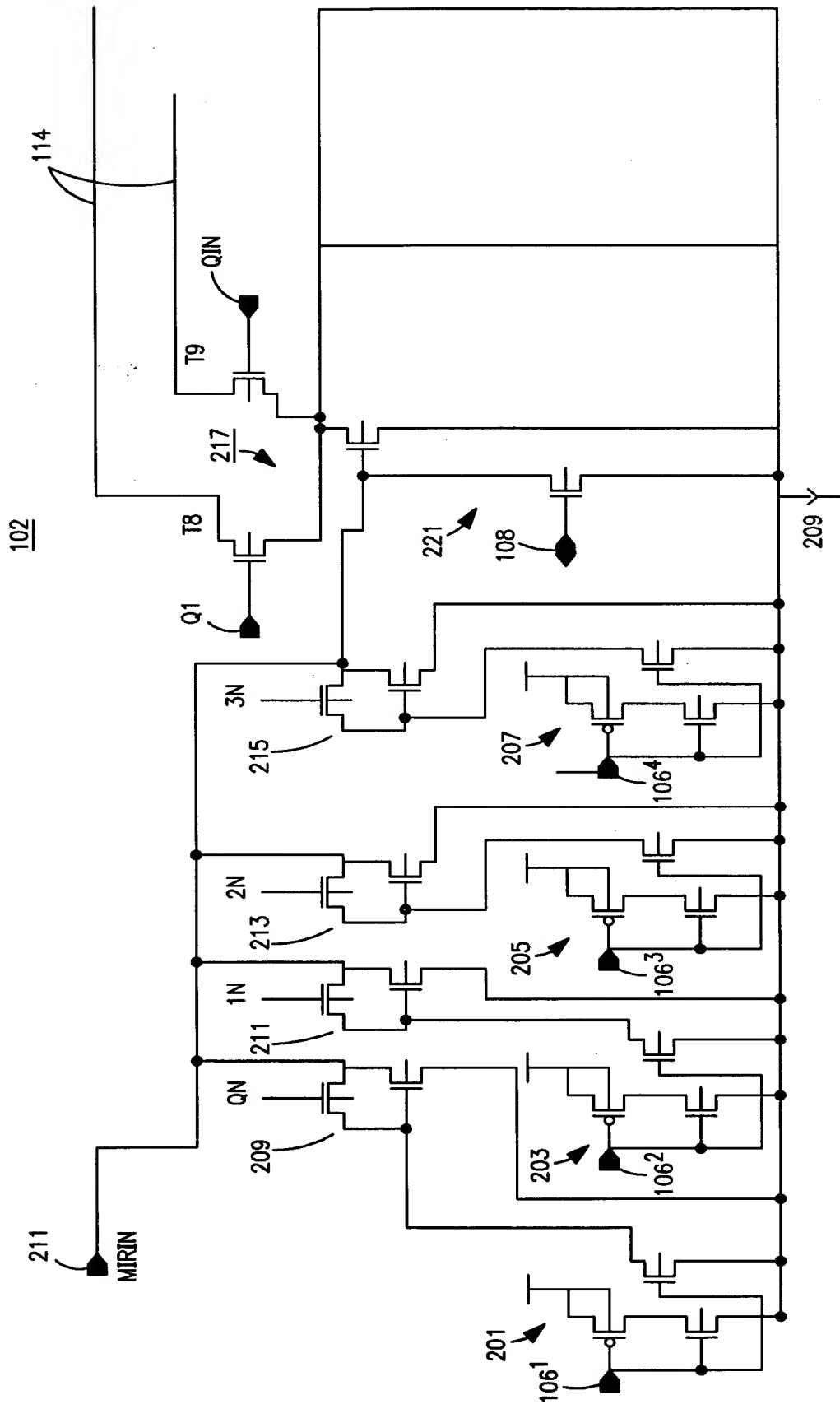


FIG. 2

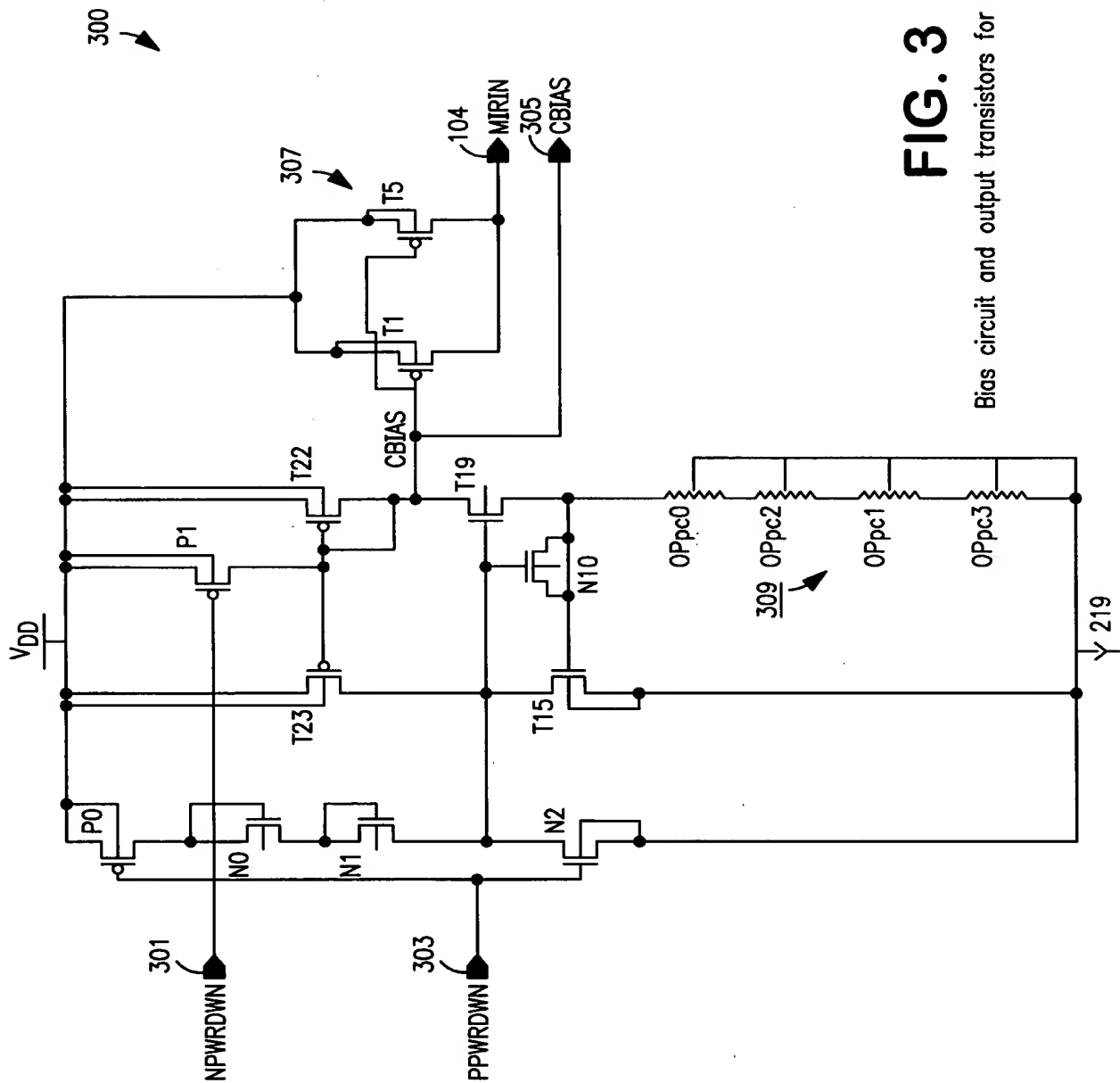


FIG. 3

Bias circuit and output transistors for FIR/driver

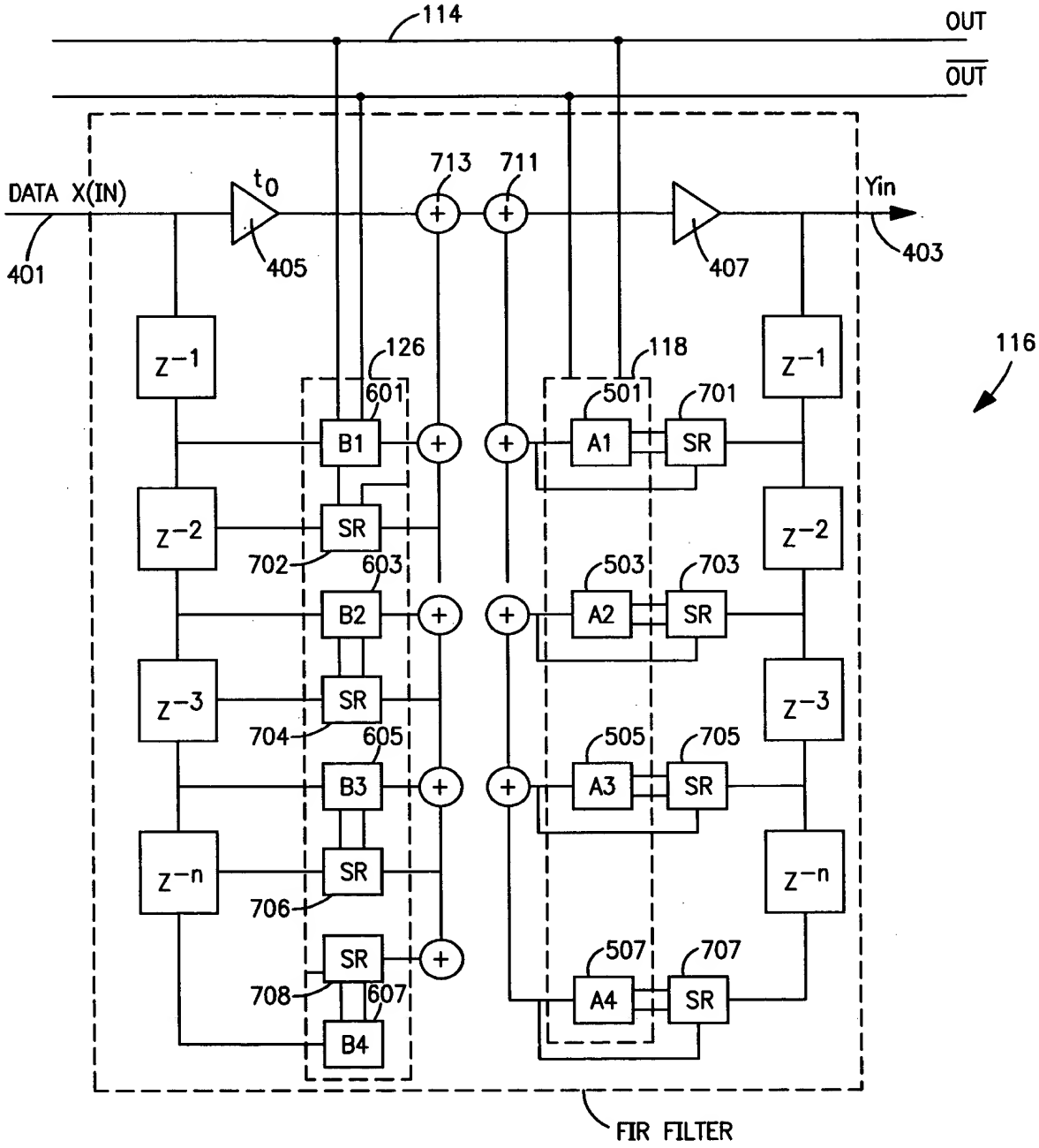


FIG. 4



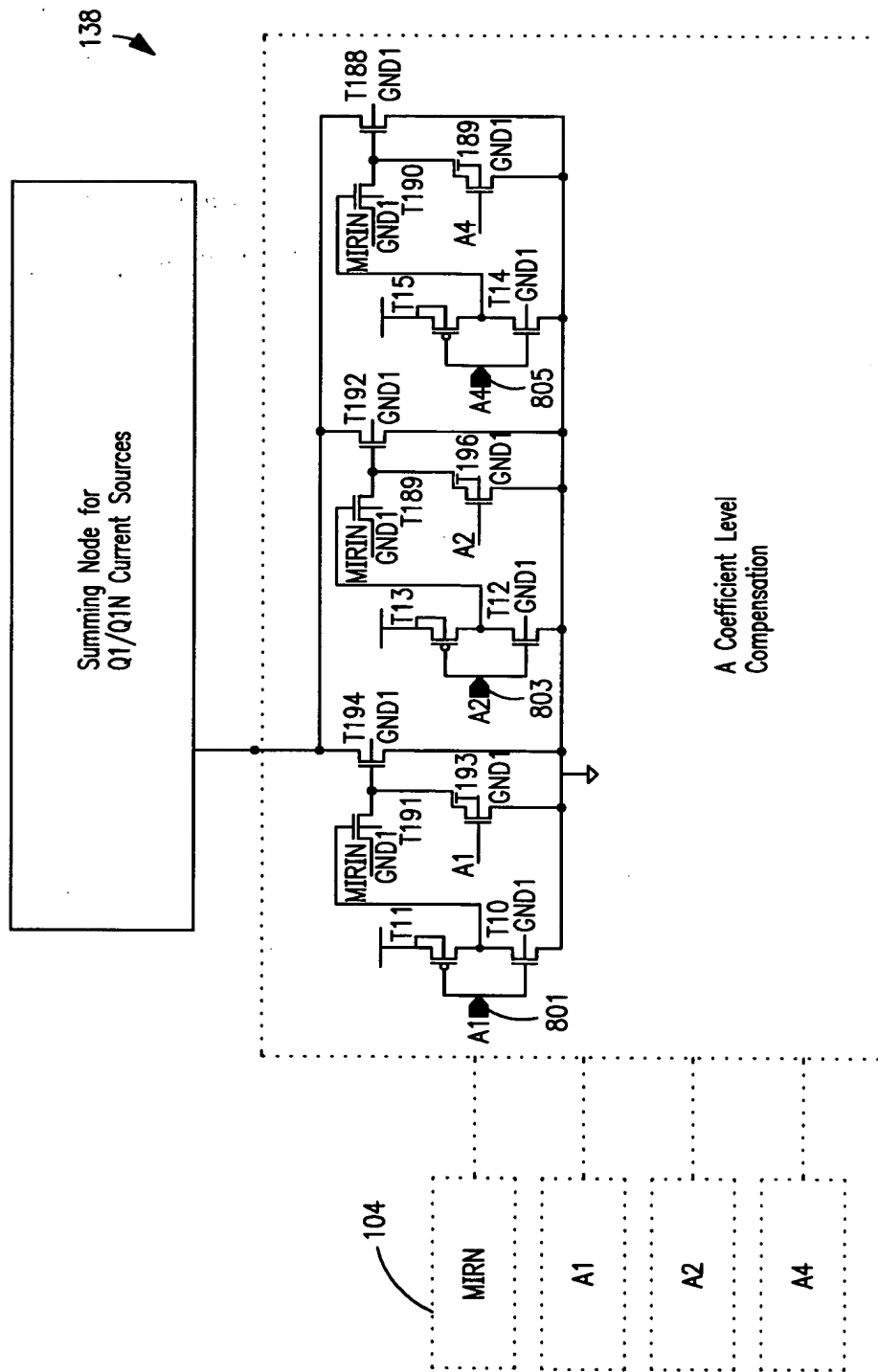




FIG. 8A

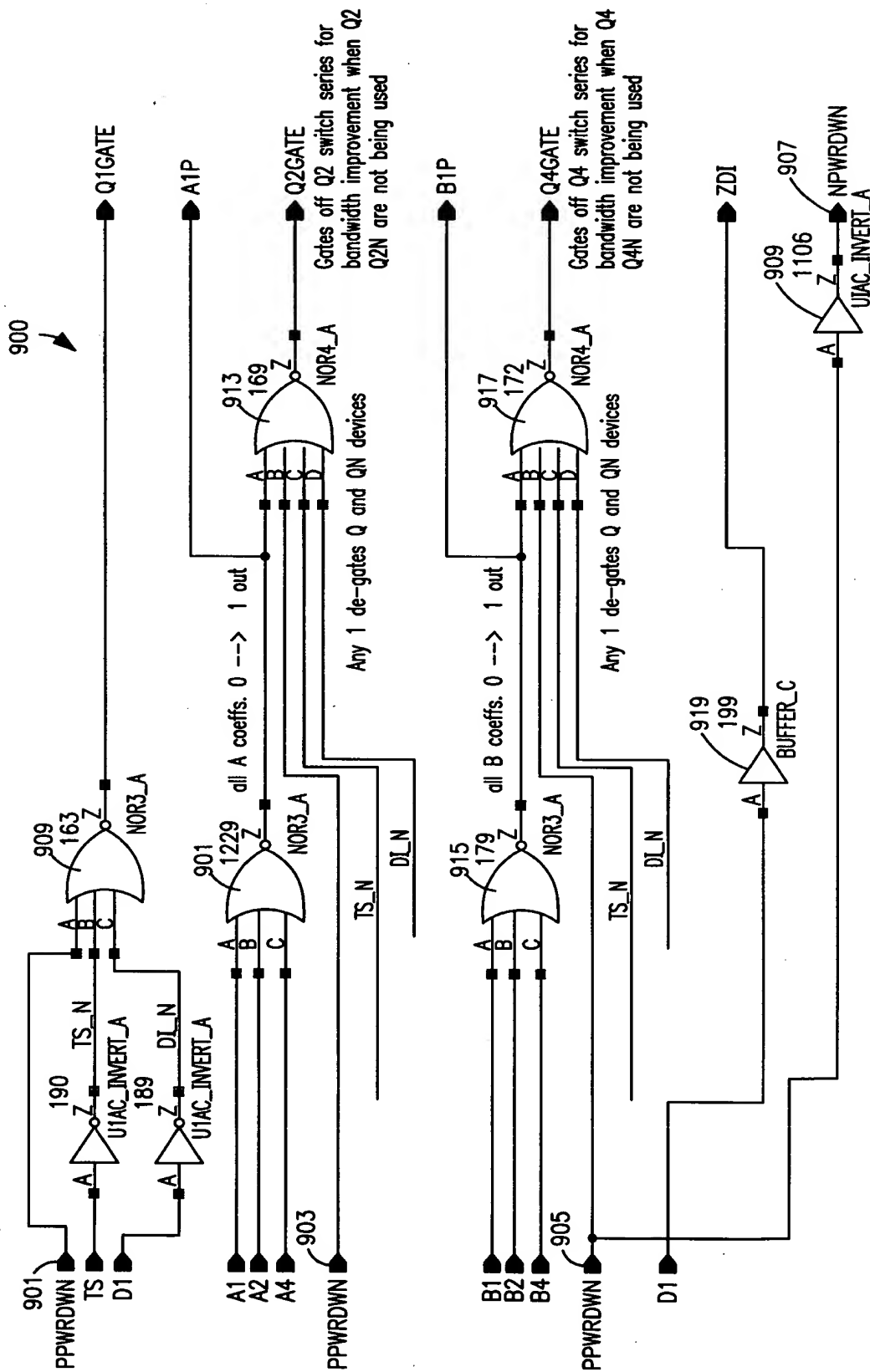


FIG. 9